## FINAL *[Week 8-12]*

## Week 8: Fabrication; Layout and Stick Diagram

1. Draw the typical cross-section of an nMOS/pMOS transistor carefully denoting each terminal and their constituent materials.
2. Draw the cross-section of a CMOS inverter in an n-well process (carefully denote each terminal and their constituent materials).
3. Draw the cross-section of a CMOS inverter in a p-well process (carefully denote each terminal and their constituent materials).
4. What are well and substrate taps and why are they necessary?
5. Describe the fabrication process steps briefly.
6. What is the photolithography process?
7. Why do we need contacts?
8. Explain briefly: CVD process, Diffusion process, Ion Implantation process.
9. Discuss some of the basic simplified rules for layout design and using the rules, derive the dimensions of an unit transistor (in terms of λ).
10. In 6 separate figures, draw the set of 6 layout layer masks (n-well, polysilicon, n+ diffusion, p+ diffusion, contact, metal) for the following CMOS inverter layout: (Fig. 1)
11. Draw the cross-sectional view of fig. 1 along Line 1 and 2.

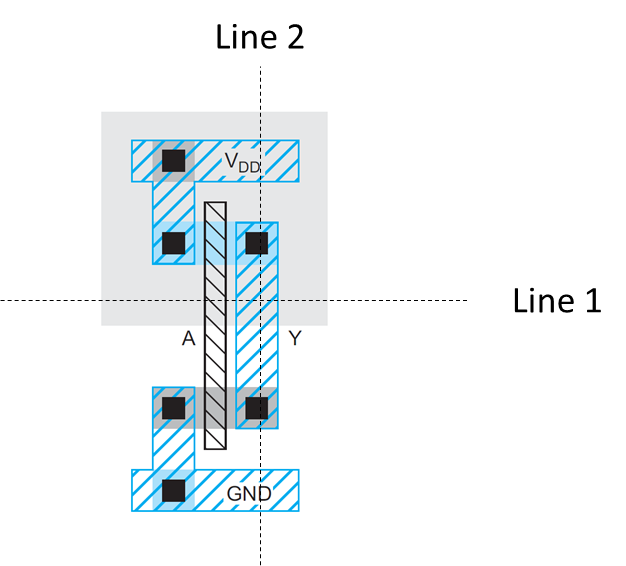
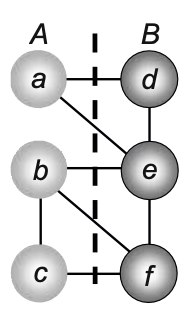


Fig. 1. Draw a set of 6 layout masks and draw the cross-sectional view

1. Briefly discuss the properties of a standard cell layout.
2. Draw the layout of an isolated nMOS/pMOS transistor.
3. Design the layout of a NAND3/NOR3 gate and determine the area.
4. Explain the "Well-spacing" rule for Lambda based design approach.
5. Define "Wiring Tracks" and derive its dimensions.
6. Explain how one can estimate the area of a layout by counting the vertical and horizontal wiring tracks from its corresponding stick diagram.
7. Practice drawing stick diagrams and estimating the area of different CMOS inverting logic functions/gates.
8. Draw the CMOS architecture and the stick diagram of the following function. Estimate the area.

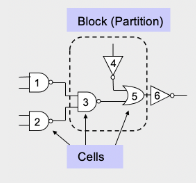
## Week 9: VLSI Physical Design-I

1. What is the difference between floor-planning and placement?
2. The graph below (nodes *a*-*f* ) can be optimally partitioned using the Kernighan-Lin algorithm. Perform the first pass of the algorithm. The dotted line represents the initial partitioning. Assume all nodes have the same weight and all edges have the same priority.

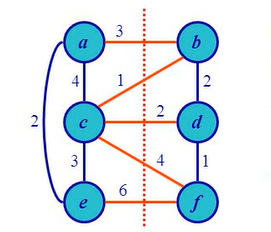


Note: Clearly describe each step of the algorithm. Also, show the resulting partitioning (after one pass) in graphical form.

1. The circuit below (nodes *1*-*6* ) can be optimally partitioned using the Kernighan-Lin algorithm. Transform the following circuit to its equivalent graph representation (**gates to nodes**) and perform the first iteration (swap) of the algorithm and compare the cut cost with the initial one. The dotted line represents the initial partitioning with block A (1,2,6) and B (3,4,5).



1. The graph below (nodes a-f ) can be optimally partitioned using the **Kernighan-Lin** algorithm. Perform the first pass of the algorithm. The dotted line represents the initial partitioning. Assume the numbers in the figure are the weights of the corresponding conections.



[Hint: Initial cut cost = 3+1+2+4+6 = 16,

Ec(a) = 3, Enc(a) = 6,

D(a) = 3-6 = -3,

D(b) = (3+1)-2 =2,

c(a,b) = 3,

g(a,b) =D(a) + D (b) - 2c(a,b) = -3 + 2 - 2.(3) = -7]

1. What are the different types of routing?
2. What are the goals of Clock Tree Synthesis (CTS)?

## Week 10: VLSI Physical Design-II( Lee's Maze Algorithm)

1. Find the shortest routing path from Source (S) to Target (T) using Lee’s Maze algorithm. Find the memory requirements for the calculation. Dark regions are obstacles or components.

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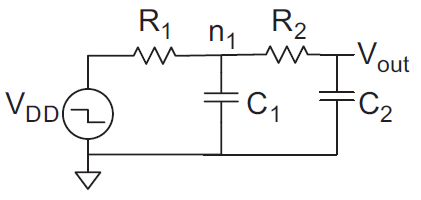
1. i. Find the shortest path for each target using lee’s maze routing.

ii. Calculate the total memory usage.

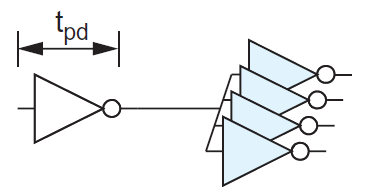
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| T2 |  |  |  |  |  |
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## Week 11: Delay

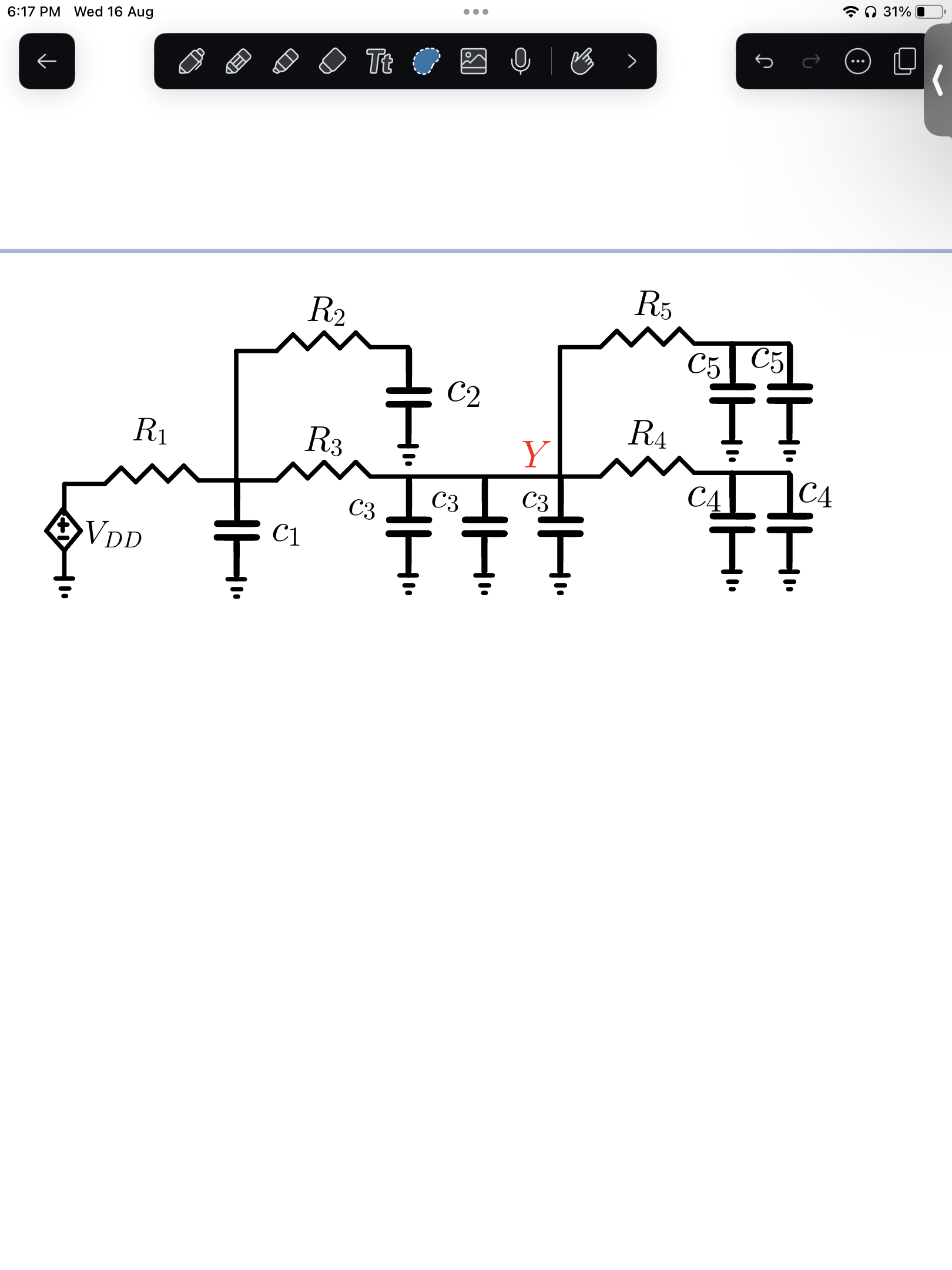
1. What are the origins of delay in CMOS circuits?
2. What are the major two delays that characterize combinational logic circuits?
3. Define tpdf, tpdr, tcdf, and tcdr using a suitable timing diagram.
4. Describe how one can compute the delay using transient response.
5. Come up with the equivalent nMOS & pMOS RC circuits for the RC delay model.
6. Sketch a 3-input NAND gate with transistor widths chosen to achieve effective rise and fall resistance equal to that of a unit inverter (R). Annotate the gate with its gate and diffusion capacitances. Assume all diffusion nodes are contacted. Then sketch equivalent circuits for the falling output transition and for the worst-case rising output transition.
7. Estimate tpdf, tpdr, tcdf, and tcdr for the 3-input NAND gate from the previous problem if the output is loaded with h number of identical NAND gates.
8. Compute the Elmore delay for Vout in the 2nd order RC system:



1. Estimate tpd for a unit inverter driving m identical unit inverters.
2. Repeat the previous problem if the driver is w times unit size.  
   If a unit transistor has R = 10 kΩ and C = 0.1 fF in a 65 nm process, compute the delay, in picoseconds, of the inverter shown with a fanout of h = 4. Repeat the problem for h = 10.



1. Exercises 4.1 4.2, 4.3, 4.4, 4.5, 4.6, 4.9, 4.18, 4.19.
2. Calculate all the propagation and the contamination delays for a 4-input NOR gate if it drives two inverter and a 3-input NAND gate. Assume all diffusion nodes are contacted and worst case rise and fall resistances are equal to that of a unit inverter (R). [Draw the circuit with gate-symbols at first and then, CMOS architecture to derive RC equivalent circuit]
3. Draw the simplified RC network and determine the expression for the Elmore delay, tpdr for node Y.



## Week 12: Power

1. A digital system-on-chip in a 1 V 65 nm process (with 50 nm drawn channel lengths and λ = 25 nm) has 1 billion transistors, of which 50 million are in logic gates and the remainder in memory arrays. The average logic transistor width is 12 λ and the average memory transistor width is 4 λ. The memory arrays are divided into banks and only the necessary bank is activated so the memory activity factor is 0.02. The static CMOS logic gates have an average activity factor of 0.1. Assume each transistor contributes 1 fF/µm of gate capacitance and 0.8 fF/µm of diffusion capacitance. Neglect wire capacitance for now (though it could account for a large fraction of total power). Estimate the switching power when operating at 1 GHz.
2. Consider the system-on-chip from the previous problem. Subthreshold leakage for OFF devices is 100 nA/µm for low-threshold devices and 10 nA/µm for high-threshold devices. Gate leakage is 5 nA/µm. Junction leakage is negligible. Memories use low leakage devices everywhere. Logic uses low-leakage devices in all but 5% of the paths that are most critical for performance. Estimate the static power consumption.
3. You are synthesizing a chip composed of random logic with an average activity factor of 0.1. You are using a standard cell process with an average switching capacitance of 450 pF/mm2. Estimate the dynamic power consumption of your chip if it has an area of 70 mm2 and runs at 450 MHz at VDD = 0.9 V.
4. You are manufacturing a chip composed of random logic and memory units with average activity factors of 0.1 & 0.05 respectively. You are using a standard cell process with an average switching capacitance of 450 pF/mm2. Estimate the dynamic power consumption of your chip if it has an area of 200 mm2 of which 60% is occupied by the logic circuit and runs at 450 MHz at VDD = 0.9 V.
5. You are considering lowering VDD to try to save power in a static CMOS gate. You will also scale Vt proportionally to maintain performance. Will dynamic power consumption go up or down?

Determine the activity factor for the signal shown. The clock rate is 1 GHz.

